Imperial College London

Lecture 3

The Anatomy of an Op-Amp

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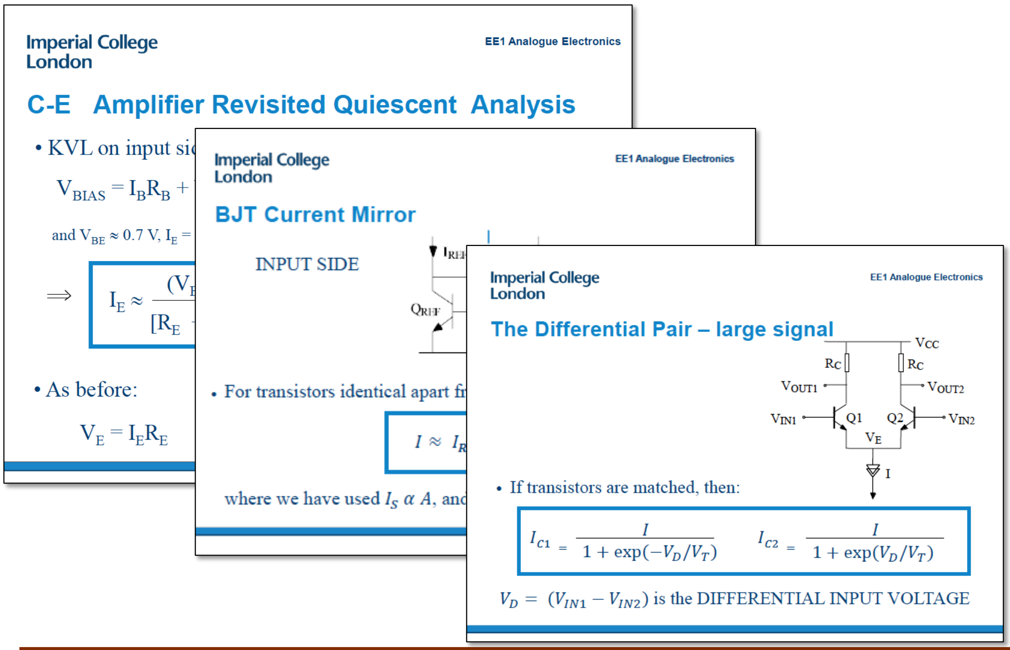
In this week's lecture, I will "dissect" the LM386 audio amplifier. The purpose of this is to expose you to what a real-life amplifier looks like inside with the packaging removed.

In Year 1, you have already learned how different types of transistor circuits work: common-emitter amplifier, differential amplifier, emitter follower etc.. You have also used SPICE to simulate, at transistor level, a typical operational amplifier as part of the Laboratory coursework.

In this lecture, we will examine in detail how the theory you explored last year is found in one of the most popular audio amplifiers used in industry. The LM386 was designed by National Semiconductors in the '70s and has remained a favourite among audio enthusiasts due to its low cost, low voltage single supply operation, minimum number of external components and low power consumption. It is particularly suitable for battery operate, portable designs.

The amplifier is built with BJTs, not FETs or MOSFETs. It is important to remember that although the LM386 contains an op-amp inside, it is NOT itself an op-amp, and it cannot be used as such.

What you should know already?

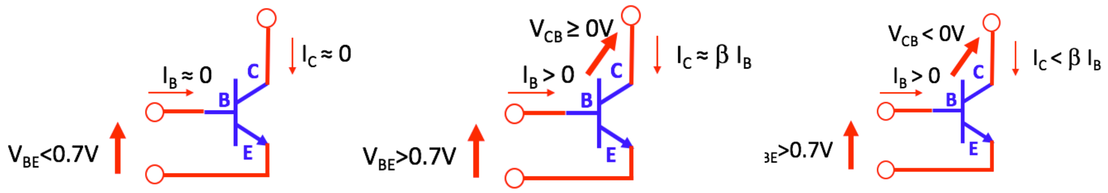


Here are extracts of some of the slices you used in the Analysis and Design of Circuits module in Year 1, where you have learned all the equations relating to currents and voltages in different configurations of bipolar transistor circuits.

While knowing equations governing the working of circuits is important, and able to analyse circuits in a rigorous manner is essential for an electronic engineer, it is also important for you acquire some intuition about circuits. Such intuitions would allow you to have deep insights on why you might consider adding a transistor at a certain place may be worth exploring. This ability would allow you to "see" how a circuit works and understand why it has limitations. This hopeful leads you inventing new circuits that work better than previous designs.

The approach taken in this lecture would therefore to minimize equations and to provide you with some "rules of thumb" that encourage such intuition.

Rules of thumb – Bipolar Junction Transistor (BJT)



- $V_{BE} < 0.7V$
- Transistor OFF
- Near zero I_B and I_C (except leakage)
- Good for digital circuits

- $V_{BE} \geq 0.7V$
- BC junction diode reverse biased
- Transistor in linear/active region
- $I_C \approx \beta\, I_B$ applies
- Good for analogue circuits

- $V_{BE} \geq 0.7V$
- BC junction diode NOT reverse biased
- Transistor in saturation region
- $I_C < \beta\, I_B$
- Good for digital circuits

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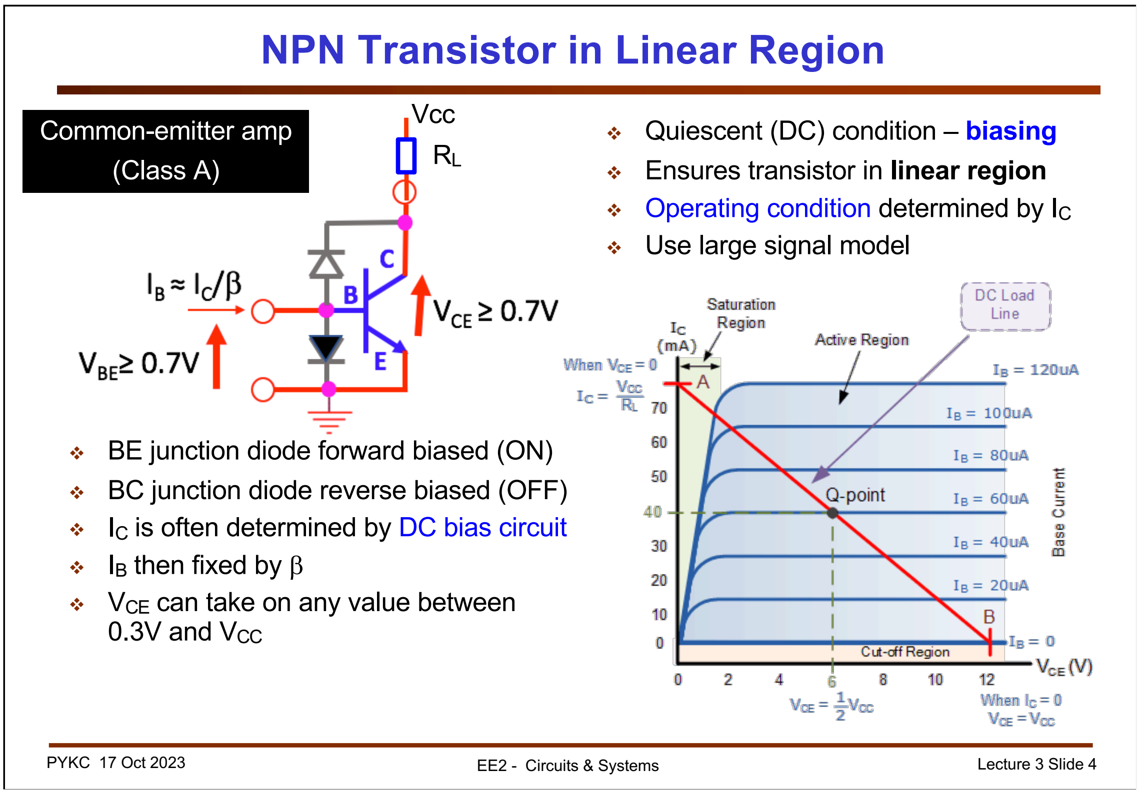
Here are some basic rules relating to bipolar transistors – NPN in this case. You should be familiar with these from Year 1, but here it is again in a condensed form.

A NPN transistor has three normal operating states:

1. **Off state** - when base-emitter voltage is lower than 0.6 – 0.7V, the base-emitter junction diode is not forward biased. The transistor is not conducting. There is nearly no current through any of its three terminals (except leakage currents). This mode of transistor is found operating in digital circuits as an OFF switch.
2. **Linear or Active state** – if the base-emitter junction diode is forward biased because $V_{BE} \geq 0.7V$ (could be lower), the transistor is conducting. Furthermore, the base-collector junction diode **must be reverse biased**. The ratio of collector current to base current is a constant (β). The transistor is operating in the linear and active region. Transistors in this state is usually found in good quality analogue circuits that are working properly.
3. **On state** – if both the base-emitter and base-collector junction diodes are forward biased, the collector-emitter voltage drops below, say, 0.3V, the transistor is in saturation mode. The collector to base current is no longer governed by β ($I_C/I_B < \beta$). The transistor behaviours like an ON switch in digital circuits.



Since we are considering analogue audio amplifiers, we are interested in transistors working in the **linear** or **active** region.

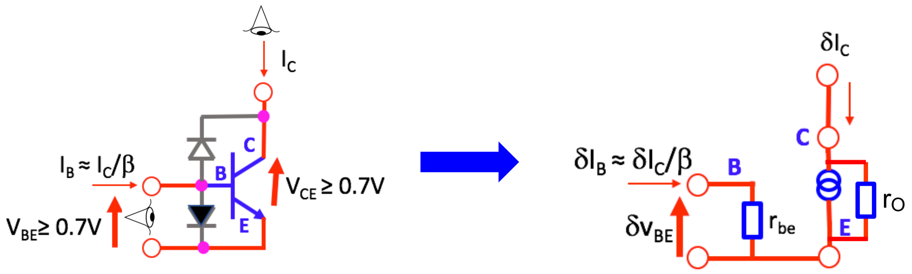
Remember again, looking into the base terminal of an NPN transistor, you see two diodes: a base-emitter diode, a base-collector diode, as shown in the slide. In this mode, the BE diode is forward biased; the BC diode is reverse biased.

To ensure that a NPN transistor is operating in the active region, one must construct circuits around the transistor such that when no signal is applied (**quiescent condition**), the transistor is operating in the required conditions. Before a transistor in an analogue circuit can do its thing (e.g. amplify signals), one must bias the transistor properly and establish all voltages and currents under DC condition (i.e. no signal).

Shown on the slide is a typical I_C vs V_{CE} characteristics of an NPN transistor. A common way to establish bias is to add a load resistor between collector and VCC. This establishes what is called a "**load line**". The idea is to bias the circuit so that under quiescent condition, the transistor "sits" at the middle of the region, which in this case is V_{CE} = Vcc/2. In this way, the output voltage at the collector will have maximum voltage swing (or range).

To ensure that the base-collector junction diode remains non-conducting, V_{CE} must not drop below 0.3V.

Small signal behaviour of NPN transistor



- Quiescent I_C determine operating point
- Small signal model – 2 resistors r_{be} and r_O, and a current source
- r_o large - can be omitted

- $\delta i_B = \delta v_{BE} / r_{BE}$
- $\delta i_C = g_m \, \delta v_{BE}$
- $\delta i_E = \delta i_B + \delta i_C$

- current gain: $\beta = \delta i_C / \delta i_B$
- transconductance: $g_m = \delta i_C / \delta v_{BE} = I_C/V_T$
- Input resistance: $r_{be} = \delta v_{BE} / \delta i_B = \beta V_T/I_C$

Once a transistor is properly biased at DC, we can consider the operation of the transistor when we inject a signal. For this, we use a simplified small signal model.

For a BJT transistor, the small signal model have parameters that are governed by the operating point of the BJT (i.e. the bias condition), particularly the value of I_C.

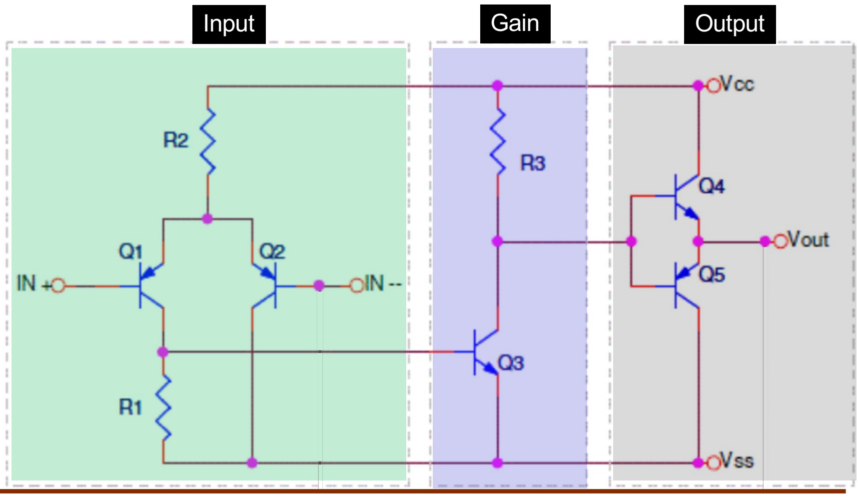
The small signal consists of an input resistance r_{be} as viewed from the base-emitter port, a voltage controlled current source between base and emitter, and an output resistance r_O in parallel with the current source between collector and emitter. Usually r_O is large enough to be removed from the model.

The three most important parameters for a NPN BJT are as shown:

1. **Current gain** β - typically 20 to 200, determined by the fabrication process;
2. **Transconductance** g_m – depends on collector bias current I_C;
3. **Input resistance** r_{be} – depends on both collector bias and property of the transistor.

Inside a typical op-amp

- Three stages architecture:
  1. **Differential input stage** – long-tail pair (Yr 1 Circuits part 2, adc_9, slides 8-14)
  2. **Voltage gain stage** – common emitter amp (adc_6, slides 3-7)
  3. **Output drive stage** – push-pull circuit



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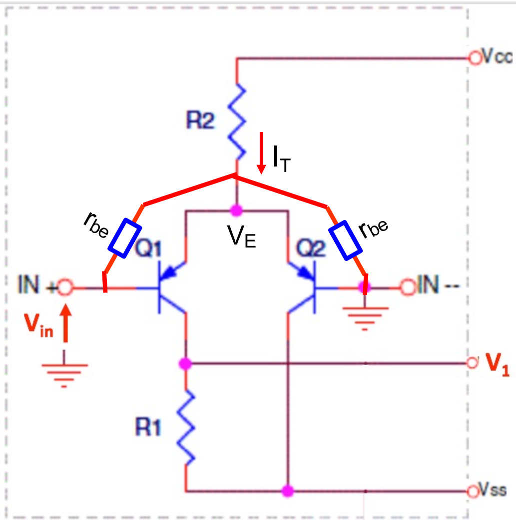
Let us now turn our attention to a generic op-amp architecture. You have already encountered this in Year 1 Spring Term Lab ADC_4, when you simulated an op-amp at transistor level using SPICE.

A typical op-amp consists of three stages:

1) The input stage provides differential inputs IN+ and IN- and gives the op-amp the ability to reject common-mode signals. (Common-mode signal is a signal that is applied to both IN+ and IN- simultaneously.)
2) The second stage is a common-emitter gain stage that provides most of the gain in an op-amp.
3) The third stage is the output stage that provides the output current capability.

In the following slides, we will examine how each stage works, and derives the gain equation from an intuitive perspective.

Differential Input Stage – differential gain



$A_{Vdiff} = \delta v_1 / \delta v_{in} = -½\, g_m * R_1$

Consider $V_{in} = 0$, IN - is grounded

- $V_E \approx 0.7V$
- $I_T \approx (V_{CC} – 0.7) / R_2$
- $I_1 \approx I_2 \approx ½\, I_T \approx ½\, (V_{CC} – 0.7)/ R_2$
- $V_1 = R_1 * I_{C1} + V_{SS}$

Apply small input signal δV_{in}

- $\delta v_E \approx ½\, \delta v_{in}$
- $\delta\, i_T \approx ½\, \delta v_{in} / R_2 \approx 0$
- $\delta\, i_1 \approx -\, \delta\, i_2 = -\, g_m * ½\, \delta v_{in}$
- $\delta\, v_1 = R_1 * \delta\, i_1 = -\, R_1 * g_m * ½\, \delta v_{in}$

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This circuit is called a “long-tail pair”, and it consists of two transistors Q1 and Q2, with a tail resistor R2, and load resistor R1.

Let us first consider the quiescent (DC) condition when both IN+ and IN- are connected to ground.

1. V_E, the emitter voltage of Q1 and Q2, is around 0.7V above ground. This determines the tail current I_T and establishes bias condition for Q1 and Q2.
2. Since Q1 and Q2 matched, their currents MUST be identical. Therefore $I_1 = I_2 = ½\, I_T$.
3. R1 can then be chosen to determine the bias voltage of the output V_1.

For differential input, assuming that signal is small at IN+ and is δV_{in}.

Viewing from IN+ terminal, the input looks like two resistors r_{be} in series to ground. These works as a voltage divider such that

$$\delta V_{BE2} = -\delta V_{BE1} = \delta V_E = ½\, \delta V_{in}$$

Since $\delta V_E << V_E$ because V_E is fixed by V_{BE2}, I_T is essentially unchanged (i.e. $\delta I_T \approx 0$).

The change in Q1 current, δI_{C1},is determined by its transconductance:

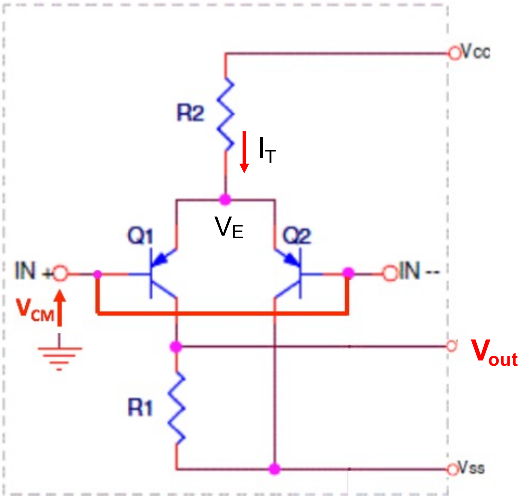
$$\delta I_1 \approx -\delta I_2 = -\, g_m * ½\, \delta v_{in}.$$

Hence, we can calculate the differential voltage gain from V_{in} to V_1 as:

$$A_{Vdiff} = -\, ½\, g_m * R1$$

To increase differential gain, we have to either increase g_m (by reducing R2, thus increasing I_{C1}) or R1.

Differential Input Stage – common mode gain



Apply v_{CM} to both inputs

- $\delta v_E \approx v_{CM}$
- $\delta i_T \approx - \delta v_E/R_2 = - v_{CM} /R_2$
- $\delta i_{C1} \approx \delta i_{C2} = ½ \delta i_T = - ½ v_{CM} /R_2$
- $\delta v_{out} \approx - R_1/2R_2 * v_{CM}$

$A_{Vcm} = \delta v_{out} / v_{CM} = - R_1/2R_2$

A good differential amplifier should amplify differential signals WITHOUT amplifying common-mode signal. Therefore we need to consider the common-mode gain of the long-tail pair circuit. For this, we connect IN+ and IN- together to a common voltage V_{CM}.

The input signal V_{CM} is transfer directly to the emitter of Q1, Q2 since V_{BE} of Q1 and Q2 remain more or less fixed at 0.7V. Therefor the tail current changes by:

$$\delta i_T \approx - \delta v_E/R_2 = - v_{CM} /R_2$$

Since both Q1 and Q2 have the same V_{BE} and they are matched, their collector currents must be identical. Hence

$$\delta i_{C1} \approx \delta i_{C2} = ½ \delta i_T = - ½ v_{CM} /R_2$$

Therefore the change in the output voltage is simply:

$$\delta v_{out} \approx - R_1/2R_2 * v_{CM}$$

From this we calculate the common-mode gain to be:

$$A_{Vcm} \approx \delta v_{out} / v_{CM} = - R_1/2R_2 \quad \text{and}$$

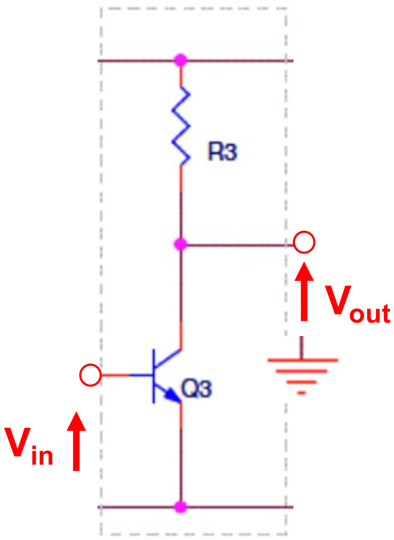
$$A_{Vdiff} \approx - ½ g_m * R1$$

Common-Mode Rejection Ratio = Differential Gain/Common-mode Gain

$$CMRR = A_{Vdiff} / A_{Vcm} \approx g_m * R_2$$

Here we illustrate a contradiction: for larger CMRR, R2 needs to increased. However, for large differential gain, we want to increase g_m and I_{C1}, which means R2 should be reduced. This contradiction limits the differential gain of the input stage.

Small Signal Gain stage



- Common Emitter amplifier (Yr 1st ADC part 2 Lecture 6, S7)
- $\delta v_{out} = - g_m \, \delta v_{in} * R_3$
- $A_V = \delta v_{out} / \delta v_{in} = - g_m R_3$
- Increase g_m and R_3
- Most of the voltage gain produced by this stage

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Due to the contradictory requirements of differential and common-mode gains, op-amp uses a second stage of amplification to provide high open-loop voltage gain. The second stage is a simple common-emitter stage with a single transistor. The gain of this stage is straight forward.

The input signal is applied directly to the base-emitter junction:

$$\delta V_{be} = \delta V_{in}$$

The NPN transistor "translates" this base-emitter voltage change to a change in collector current determined by the transconductance parameter g_m.

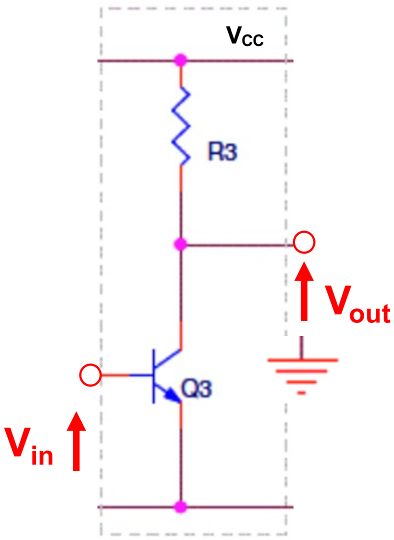
The overall voltage gain of this stage is therefore:

$$A_V = \delta v_{out} / \delta v_{in} = - g_m R_3$$

To increase stage 2 gain, one can increase g_m by increasing the bias current to Q3, and/or increase the load resistance R3.

Unlike the input differential stage, this stage has no impact on CMRR and there is no restriction (at least in theory) to the gain of this stage. As a result, most of the voltage gain is obtained from this 2nd stage.

Gain stage is not suitable to drive output load



- Common-emitter amplifer is also called a **Class A amplifer** (name does not matter)
- R3 is the load (e.g. speaker)
- Transistor Q3 works throughout the entire cycle of a sine signal (360º)
- Very poor power efficiency:

$$efficiency\ \eta = \frac{power\ to\ load\ R_3}{Power\ from\ supply} < 25\%$$

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The gain stage with common-emitter (CE) configuration is also known as a class A amplifer. The name does not matter. What it means is that, assuming we are amplifying a sinewave signal, the transistor Q3 is conducting throughout the entire cycle of a sinewave.

It is a common-emitter configuration because the emitter is common to both input Vin and output Vout.

Why do we need a 3rd stage in an op-amp to drive an output load? Could we not simply use R3 as the output load, for example driving a speaker directly?

The answer is that this circuit is extremely inefficient. It takes a lot of power from the supply rail (Vcc) to deliver useful power to the output (R3 in this case).

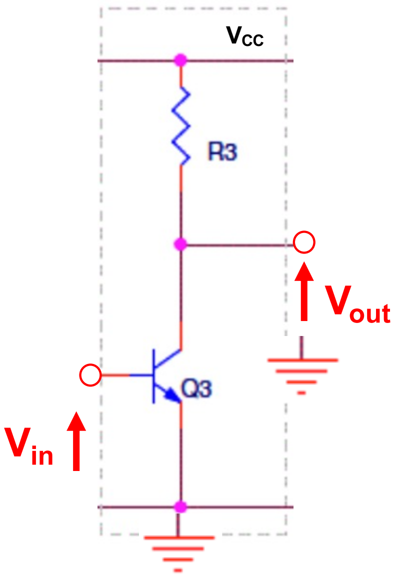
The efficient of a power amplifier is defined as the ratio:

$$efficiency\ \eta = \frac{power\ to\ load\ R_3}{Power\ from\ supply}$$

Here, the signal is assumed to be sinusoilal.

In the next slide, it will be shown that even for the best case scenario, the power efficiency of a class A amplifier is at most 25%. In most case, this could be a lot less!

Efficiency of a class A amplifier



- Assume Vout at quiescent (i.e. no input) is biased to be at Vcc/2
- Quiescent collector current I_{CQ} = (Vcc/2)*R3
- Average power drawn from supply voltage is:

$$P_i(dc) = V_{CC}\ I_{CQ} = \frac{{V_{CC}}^2}{2 * R3}$$

- AC power delivered to load R3 is:

$$P_o(ac) = \frac{V_{out}(rms)^2}{R3}$$

- P_o is maximum when $V_{out(pk-pk)}$ = V_{CC}, i.e. maximum output voltage swing
- Or $V_{out}(rms)$ = $V_{CC}/2\sqrt{2}$
- Therefore max $P_o(ac) = \frac{{V_{CC}}^2}{8R3}$
- Hence max $\eta = \frac{maximum\ \ P_o(ac)}{P_i(dc)} = \frac{{V_{CC}}^2/8R3}{{V_{CC}}^2/2R3} = \frac{1}{4}$

To calculate the efficiency, consider the best quiescent condition, which is when Vout is at Vcc/2. The output is capable of providing maximum output swing. On average the amplifier will raw a current of Vcc/(2*R3). Therefore the DC supply power is Vcc^2/(2R3). Even if the output is NOT swing (i.e. not delivering any output power), this is the power that supply source would need to provide.

Now the output power is maximized when Vout swings from 0V to Vcc. That is, the output has peak-to-peak voltage of Vcc.

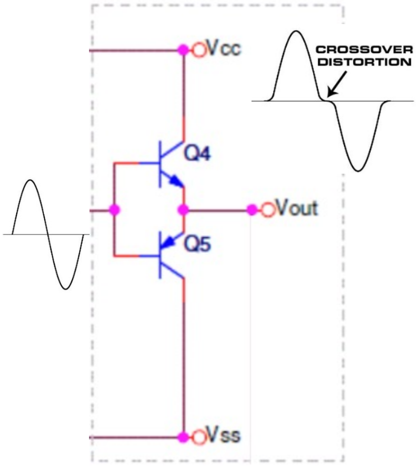
Even in this best-case condition, the RMS voltage of the output is amplitude divide by $\sqrt{2}$. Therefore the best case output voltage is Vcc/ 2$\sqrt{2}$.

Therefore the best case efficiency is ¼, or only 25%!

This is of course is very inefficient way to deliver power to a load.

As a result, amplifiers designed to drive a load would use a different output driving stage as shown in the next slide.

Output Stage



- Yr 1[st] ADC part 2 Lecture 6, S3-5
- Q4 is emitter follower (Common-Emitter) for sourcing current to Vout (PUSH)
- Q5 is another emitter follower for sinking current from Vout (PULL)
- This is known as a PUSH-PULL or class B amplifer circuit
- $\delta Vout \approx \delta V_{in}$, i.e. its gain is 1
- Each transistor only operate for half cycle or 180º of a sinewave signal
- Further, Q4 and Q5 requires VBE > 0.7V to start conducting, therefore this amplifier has distortion.

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The third stage consists of complementary transistors Q4 and Q5. They each acts as an emitter follower circuit for the positive and negative half of V_{IN} (as a sine wave) relative to the quiescent condition of V_{out}. This circuit structure is known as the "Push-Pull" configuration or a class AB amplifier.

If $V_{in} \geq V_{out}$(quiescent) + 0.7V, Q4 provides current to drive V_{out} to $V_{in} - V_{BE4}$. This is known as "push" action - it sources current to the output load.

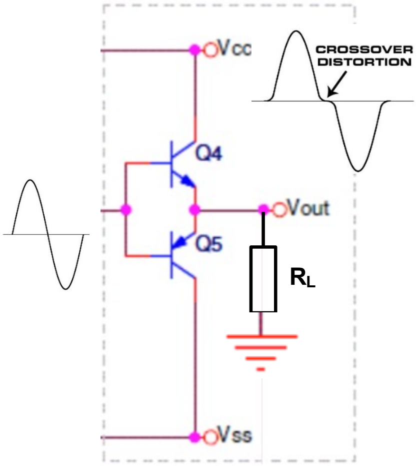
If $V_{in} \leq V_{out}$(quiescent) - 0.7V, Q5 absorbs current to drive V_{out} to $V_{in} + V_{BE5}$. This is known as "pull" action - it sinks current from the output load.

This circuit incurs significant distortion when $-0.7 \leq V_{in} \leq +0.7$. During such crossover region, neither Q4 nor Q5 is conducting and the output is not effectively driven. Therefore this amplifer always causes distortion at the crossover.

The small signal voltage gain of the 3[rd] stage is approximately 1.

This push-pull amplifier is also known as a class B amplifier. It is inherently more efficient than a class A amplifer, as will be seen in the next slide.

Push-pull (Class B) amplifier efficiency



- Assume Vss = -Vcc for simplicity, output swing is $\pm V_{pk}$ and V_{pk} = Vcc.
- Q4 and Q5 conduct only for half cycle, hence

  DC supply power $P_i(dc) = V_{CC}\, I_{DC}$
- Average current is that of a full-wave rectified signal: $I_{DC} = \frac{2}{\pi} I_{pk}$ where I_{pk} is the peak output current.
- Hence $I_{DC} = \frac{2}{\pi}\left(\frac{V_{pk}}{R_L}\right)$, and $P_i(dc) = \frac{2}{\pi}\left(\frac{V_{CC}^2}{R_L}\right)$
- Output AC power is (from before)

$$P_o(ac) = \frac{{V_{out(pk-pk)}}^2}{8R_L} = \frac{(2V_{pk})^2}{8R_L} = \frac{{V_{CC}}^2}{2R_L}$$

- Hence $\eta = \frac{P_o(ac)}{P_i(dc)} = \frac{V_{CC}^2/2R_L}{\frac{2}{\pi}\left(\frac{V_{CC}^2}{R_L}\right)} = \frac{\pi}{4} = 78.5\%$

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To simplify the calculation, let us assume that we are using dual power supply and Vss = - Vcc. Also the output is driving a resistive load R_L.

The output voltage is swinging between +Vpk and –Vpk, and for simplicity, is assume to be $\pm$Vcc.

Now the current drawn from either Vcc or Vss supply for half of a sinewave or each supply rail because only one of Q4 or Q5 is conducting at any one time. The RMS current is (simple integration) is $\frac{1}{\pi} I_{pk}$ each, or $\frac{2}{\pi} I_{pk}$ in total (one from each supply).

$$I_{pk} = \frac{V_{pk}}{R_L}$$

Therefore the input DC power from supply is:

$$P_i(dc) = \frac{2}{\pi}\left(\frac{{V_{pk}}^2}{R_L}\right) = \frac{2}{\pi}\left(\frac{{V_{CC}}^2}{R_L}\right)$$

The output AC power is as shown in the slide:

$$P_o(ac) = \frac{{V_{out(pk-pk)}}^2}{8R_L} = \frac{(2V_{pk})^2}{8R_L} = \frac{{V_{CC}}^2}{2R_L}$$

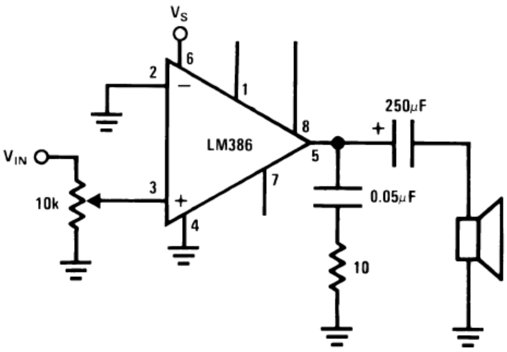
The power efficiency is therefore $\eta = \frac{P_o(ac)}{P_i(dc)} = \frac{\pi}{4} = 78.5\%$

This is much higher than the 25% best case found with Class A amplifier.

Driving 8Ω speaker with LM386

LM386
Low Voltage Audio Power Amplifier

Amplifier with Gain = 20
Minimum Parts



Features

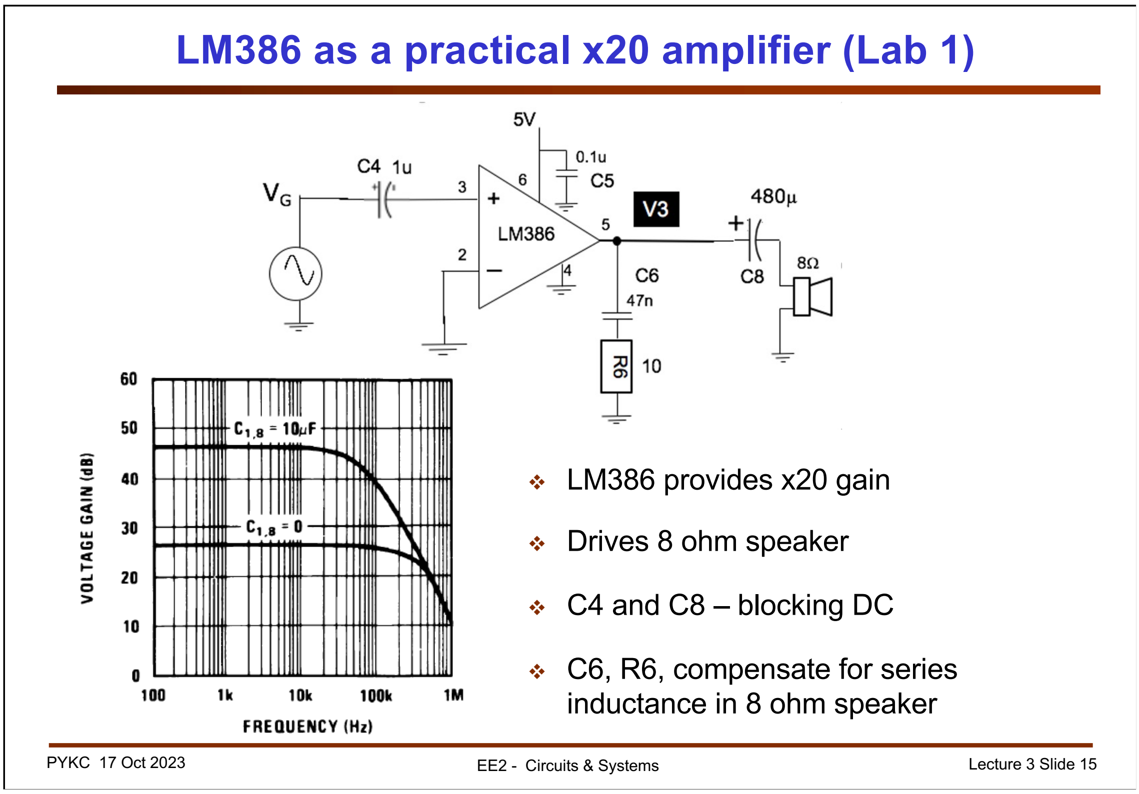
- Battery operation
- Minimum external parts
- Wide supply voltage range: 4V–12V or 5V–18V
- Low quiescent current drain: 4mA
- Voltage gains from 20 to 200
- Ground referenced input
- Self-centering output quiescent voltage
- Low distortion: 0.2% (A_V = 20, V_S = 6V, R_L = 8Ω, P_O = 125mW, f = 1kHz)
- Available in 8 pin MSOP package

In Lab 1, you will be using the LM386 audio amplifier (special op-amp designed just to drive speakers) to produce sound on an 8 ohm speaker.

This is necessary because the MCP6002 op-amp that you were using can drive around 10mA load current – no where large enough to drive the speaker.

Understanding how the detail transistor level circuit works inside an LM386 is not required in this 2nd year module. However, for those who are interested in the details, a separate, non-examinable, document explaining the circuits inside an LM386 is available on the course webpage.

The output stage of the LM386 is a modified Class B amplifier (push-pull) which eliminate most of the crossover distortion. This amplifier architecture is known as class AB amplifier – but who cares about what it is called! You may read the supplementary notes which explains how it works.



In Lab 1, you will build a x20 amplifier driving an 8 Ω speaker.

C4 and C8 provide AC coupling for both input and output signals.

The input capacitor C4 prevents the signal source from disturbing the DC bias for the LM386.

The output capacitor C8 prevents the output offset of $V_{CC}/2$ being applied to the speaker, which may result in damage to the load.

The speaker is NOT equivalent to just an 8 Ω resistor. The voice coil of the speaker has an equivalent circuit of an inductor in series with a resistor. As a result, the load impedance changes with frequency, with the loading increases at higher frequencies. This can result in the phase of the output signal changes at higher frequencies in such a way that the internal feedback can cause oscillation to occur. C6 and R6, the series RC network at the output provides compensation and avoid instability.